

## Basic Steps to Successful EMC Design

*Solid design techniques and common sense are your best tools to reduce the effects of electrical and thermal stresses on electronic systems.*

By V. Lakshminarayanan

The effects of electromagnetic interference (EMI), electrostatic discharge (ESD) and thermal stresses have become important areas of interest to electronic system designers. EMI, ESD and thermal stresses constitute some of the major causes of failure of electronic systems. The advent of small size portable appliances, switching power supplies, wireless transmitters and receivers, high speed semiconductor devices, etc., has created the need for solving the electrical environmental pollution caused by EMI. The increasing trend towards miniaturization in electronics has heightened concerns over ESD induced failures of electronic devices, and thermal design of compact packages to avoid thermal overstress failures. This article will address some of these issues, how to deal with them and how to increase product reliability.

### Some EMI/ESD background

EMI is generated wherever there are quick changing electric and magnetic

fields. Fluorescent lights, electric motors, medical equipment, domestic appliances such as shavers, mixers, ovens, automobile ignition circuits, etc. are all familiar sources of EMI. Further, EMI may not necessarily be man-made. Lightning discharges, for example, are major sources of EMI.

Every year thousands of electronic and telecommunications systems suffer damage due to lightning generated EMI. While much EMI is a source of nuisance, it can also cause major damage in a critical applications such as life support systems. For example, the electronics in a pacemaker could fatally malfunction under the influence of strong EMI or an electronically guided missile could go off track if EMI corrupts the signals to it. EMI also jams communication transmitters and disrupts communications links. Thusly, the potential losses arising from EMI make EMI control a necessity.

Electrostatic discharge is generated by friction between two surfaces, which causes a voltage difference between them. The static voltage can reach levels as high as 20KV under dry con-

ditions. ESD can be considered as a lightning discharge on a smaller scale. Even a simple event such as walking on a synthetic carpet can induce several kilovolts of static electricity in the human body. When such an electrically charged person comes into contact with a conducting surface, a short duration, high current discharge occurs. This ESD discharge generates high levels of RF interference (RFI) that contain spectral components covering a wide frequency range. Apart from the direct device damage caused by ESD, the smaller device geometry and surface mount devices (SMD) technology has increased the propensity for ESD damage due to the thinner device layers involved. The problem of ESD damage to electronic components will increase over the years unless appropriate awareness is applied at the design, fabrication, assembly and handling stages of the components.

### The heat is on

Next to EMI and ESD, thermal problems are a major factor affecting the reliability of electronic systems. Thermal overstress is generally a by-product of electrical overstress in electronic components. High voltage transients, large current flow, etc. can exceed the designed levels of thermal dissipation in the device and cause thermal runaway. Good design practice dictates that a mechanism should exist for the transfer of heat from the component as it is generated so that build up of heat can be avoided. There should be a path for the transfer of heat from the hot component to the ambient environment. Then thermal equilibrium will be reached when the amount of heat generated is equal to the amount of heat dissipated to the surroundings. The reliability of electronic components depends on the temperature of the device reached during operation. It is very important to keep the junction temperature of the device within safe

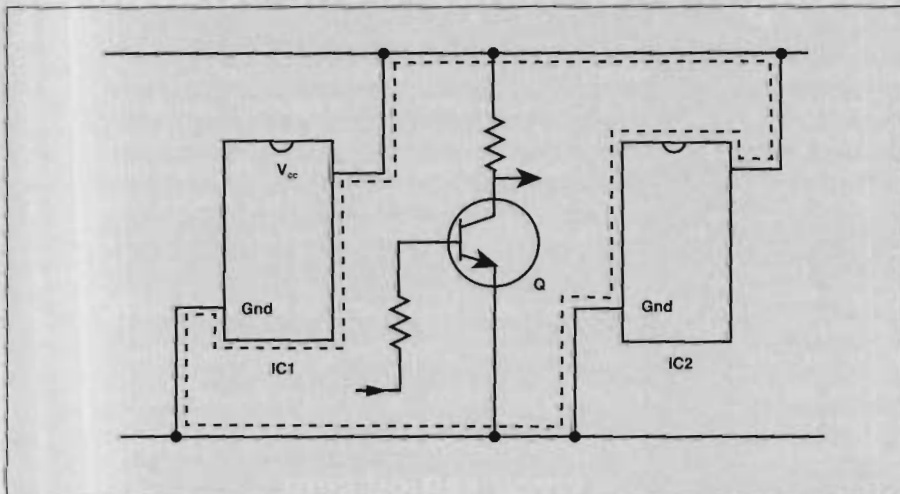


Figure 1a. A large loop area enclosed by a faulty PCB layout scheme.

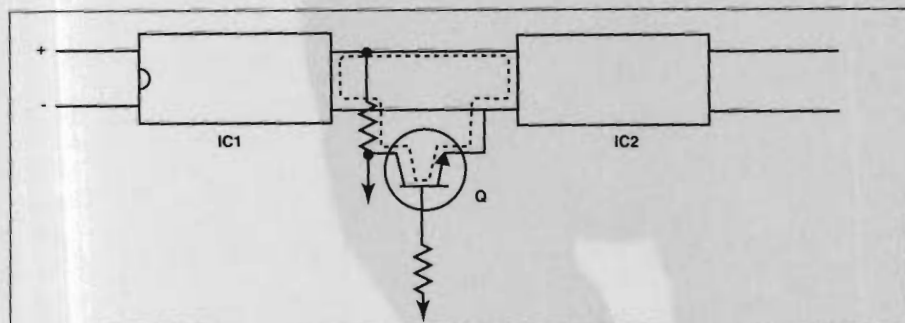


Figure 1b. A better layout technique which reduces the enclosed loop area.

limits in order to avoid device failure due to thermal overstress.

### Sources and causes of EMI and ESD

Natural sources of EMI include lightning discharges, atmospheric charges and cosmic sources, including the sun. Man-made sources of EMI include any electrical or electro-mechanical apparatus, machine tools, automobile ignition systems, communication electronics, telephony circuits, power lines, welding systems, transformers, etc.

ESD can be generated by actions such as rubbing the hands on a synthetic seat cushion, walking on a carpeted floor or simply touching charged objects. Higher humidity conditions reduce the effect of static charges by providing a discharge path to ground for the accumulated charge. Therefore, dry air conditions tend to aggravate ESD problems and humid conditions reduce charge accumulation. A typical example is shown in Table 1. The table shows the voltages generated by various human activities under 15% to 30% relative humidity conditions.

For ESD to cause any effect, there must be a generator of ESD and a receptor (component).

Materials are classified according to their tendency to give up electrons. This series is called the triboelectric series. Table 2 lists commonly used mate-

rials within the series.

The top end of the table indicates materials which are more positive (they more easily release electrons) and the materials towards the lower end of the table are more negative (they easily absorb electrons).

### EMI and ESD effects on electronic devices:

EMI becomes a nuisance in a system if there is a source of interference, a medium to transfer or couple the interfering signal and a susceptible system which will be affected by the EMI. A good design dictates that as much of the potential EMI environment be eliminated from the system during the design stage. An interfering electromagnetic signal can be conveyed from a source of EMI to a susceptible device by conduction or radiation. In conductive EMI transfer, a physical conductive path exists between the source and destination whereas in radiative EMI transfer, the EMI signal propagates through the medium from the source to the susceptible device. EMI reduction methods can be implemented in the most economical way only during the design phase of the product by choosing the appropriate methods such as using suitable circuit design techniques, proper choice of components, good PCB layout, and proper grounding and shielding methods to achieve compli-

ance with EMI standards.

The major hardware failures caused by ESD are as follows: Rupture of the thin films of oxide in semiconductor devices due to dielectric breakdown; melting of metalization traces due to high levels of thermal overstress induced by electrical overstress (EOS); current crowding effect in p-n junctions due to high current densities; latch-up in complementary metal oxide semiconductor (CMOS) devices due to parasitic pnpn structures. One must also be aware of component degradation or latent defects in the device structures which will not lead to immediate failure of the device but cause intermittent malfunctioning and field failures after exposure to ESD stress.

The ESD susceptibilities of the devices varies depending on the technology used. The range of ESD thresholds vary from 10 V to 100 V in the case of metal-oxide semiconductor field-effect transistor (MOSFET), from 300 V-7000 V in the case of bipolar devices, and from 150 V to 3000 V in the case of CMOS. ESD and EMI circuit vulnerability should be taken into account during the device selection stage.

### Circuit Design guidelines to reduce EMI and ESD effects

The following techniques will help in reducing EMI and ESD problems to a large extent.

- Use ICs with the right speed. Do not use high speed logic, unless your design needs it. Use of high speed devices will increase the problems of unwanted radiation because of the high speed of switching involved.
- Reduce slew rate of signals in analog circuits.
- Avoid fast rise time signals as much as possible.
- Use a multilayer PCB with separate ground and VCC planes if possible.
- Connect a sufficient number of decoupling capacitors from the power supply to the ground pins of ICs, very close to

| Series number | Activity                               | Typical Potential generated | Maximum Potential generated |
|---------------|----------------------------------------|-----------------------------|-----------------------------|
| 1.            | Person walking across carpet           | 12,000V                     | 39,000V                     |
| 2.            | Person walking across vinyl floor      | 4,000V                      | 13,000V                     |
| 3.            | Person working at bench                | 500V                        | 3,000V                      |
| 4.            | 16-lead DIPs in plastic box            | 3,500V                      | 12,000V                     |
| 5.            | 16-lead DIPs in plastic shipping tubes | 500V                        | 3,000V                      |

Table 1.

the IC's supply pin.

- Use feedthrough capacitors at entry/exit points in the system enclosure.
- Use differential mode signal routing to achieve cancellation of mutual inductance and common mode effects.
- Terminate strip lines with appropriate

impedance to prevent signal reflections.

- Use ferrite beads to unshielded wires to suppress EMI.
- Edge-triggered devices are prone to false triggering from ESD transients. Avoid if possible.
- Do not leave unused pins of an IC

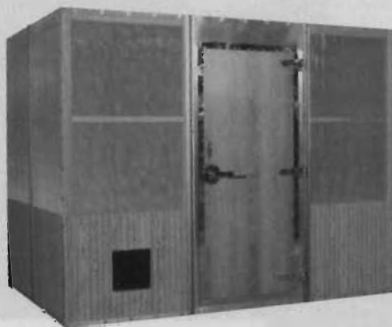
| Series Number | Material       |
|---------------|----------------|
| 1.            | Dry Air        |
| 2.            | Human skin     |
| 3.            | Bakelite       |
| 4.            | Glass          |
| 5.            | Mica           |
| 6.            | Human hair     |
| 7.            | Nylon          |
| 8.            | Wool           |
| 9.            | Silk           |
| 10.           | Aluminum       |
| 11.           | Paper          |
| 12.           | Wood           |
| 13.           | Steel          |
| 14.           | Rubber         |
| 15.           | Epoxy glass    |
| 16.           | Copper, Nickel |
| 17.           | Silver, Brass  |
| 18.           | Gold, Platinum |
| 19.           | Polystyrene    |
| 20.           | Polyester      |
| 21.           | Polyethylene   |
| 22.           | PVC            |
| 23.           | Silicon        |
| 24.           | Teflon         |

Table 2.

floating. Such pins can pick up noise which can affect the state of the device and cause spurious operation. Unused pins should be tied low or high depending on the design.

- Use a level sensing logic with a validation strobe to improve ESD immunity of the circuit. Parity and frame error checking should be used in the design to minimize errors.
- Keep all component leads short. Lead inductances and parasitic can cause cross-talk, higher propagation delays and oscillations at higher frequencies.
- When selecting components, consider the bandwidth, rise and fall times, switching speeds, voltage swing, power handling capability, immunity of the device threshold to ESD damage, and similar factors.
- If shielded cables are used ensure that a full 360° contact with the shield is made to prevent antenna effects i. e., radiated fields. Follow all packaging guidelines as applicable to EMI reduction.
- Avoid protrusion of component leads in PCBs. Trim the component leads to the minimum level required for mechanical strength.
- Electrolytic capacitors have higher series resistance and are not recommended for higher frequencies. Mica and ceramic feedthrough capacitors are recommended for frequencies > 1

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MHz. A feedthrough capacitor provides suppression of unwanted electromagnetic interference signals at the boundary between an equipment and its surroundings. In this capacitor, the EMI signals are bypassed to ground at the interface and thus prevented from crossing the boundary.

- Components mounted on heat sinks which are to be connected to the chassis for better thermal design, should have a Faraday screen to avoid capacitive coupling.
- Use ferrite beads at critical points in the circuit. A ferrite bead can be used to suppress high frequency interfering signals above 1 MHz without affecting the low frequency performance of the circuit where it is used. A typical ferrite bead adds a few  $\mu\text{H}$  of inductance to the wire in which it is slipped on. Since a ferrite bead need not be directly connected into the circuit, it is advantageous in many applications.
- A series resistor can be connected to the input stage of a high impedance circuit to limit the inrush current from an ESD transient.
- Use a small value ceramic capacitor to decouple sensitive points in the circuit to ground. Such capacitors should be mounted very close to the pin. Avoid long trace lengths which can induce parasitics.

#### Minimizing catastrophic failures :

In some situations it may not be pos-

sible to provide total protection against all contingencies. In such cases it is preferable to provide protection to the extent possible and use circuit design techniques to provide a systematic shutdown of the processes at the instant of failure of the system. This means a system can go into a graceful shutdown instead of an abrupt failure. Such features can be incorporated through software techniques so that if a sudden power fault occurs, a power monitor resets the processor so it doesn't enter a faulty program execution stage and the whole system goes away. In such situations, good hardware and software design can help cope with voltage transients and other problems without large-scale damage. Therefore, both hardware as well as software techniques can be used to avoid catastrophic failure of systems due to ESD or EMI problems.

#### Reducing EMI from transformers and switched mode power supplies

By their nature, transformers constitute one of the major EMI sources in electronic systems. In the case of switching circuits such as switched mode power supplies, motor drives, etc., the problem gets accentuated due to fast changing electric and magnetic fields. Usually the switching waveforms are rectangular pulses and a Fourier analysis of the spectrum of such a waveform shows that it is rich in harmonics. This creates a large fre-

quency spectrum of interference. The EMI in such a case will be both conducted and radiated.

Conducted mode EMI consists of two types; common mode voltage and differential mode voltage. Common mode voltage is the voltage appearing between any of the input, output or supply lines with respect to the ground. Differential line voltage is the voltage appearing between any two input, output or supply lines.

Typical EMI sources in a switching power supply are :

- radiation from the power supply circuits
- noise from the output stages of the power supply
- current changes in the rectifier diodes at high frequency can cause rapid  $di/dt$  transitions.
- high frequency switching of transistors, MOSFETs, etc.
- input/output coupling with poor isolation.
- radiated fields from coils, transformers, etc.

To reduce the effects of these, several techniques can be used in a switched mode power supply design. Some are filters, shielding techniques or even a different design approach using a sinusoidal waveform instead of a square waveform to address the harmonic problem.

#### Reduce EMI and ESD effects using sound PCB design techniques

The design of a printed circuit board

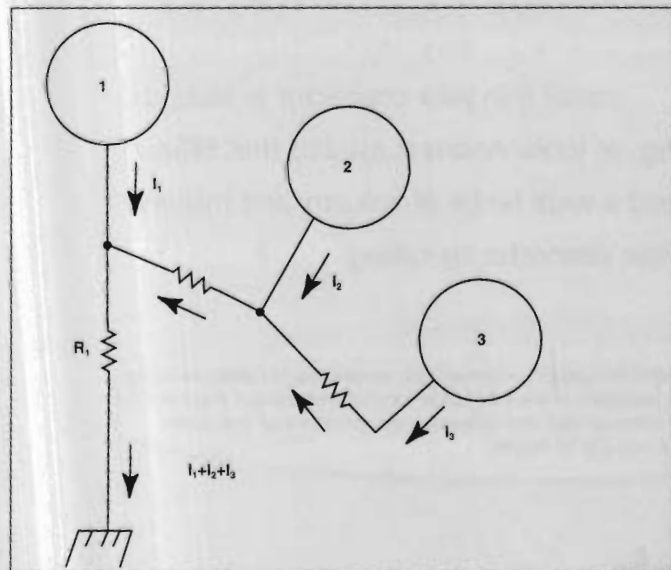


Figure 2a. A daisy-chain grounding scheme causes local voltage drops and introduces common impedance paths.

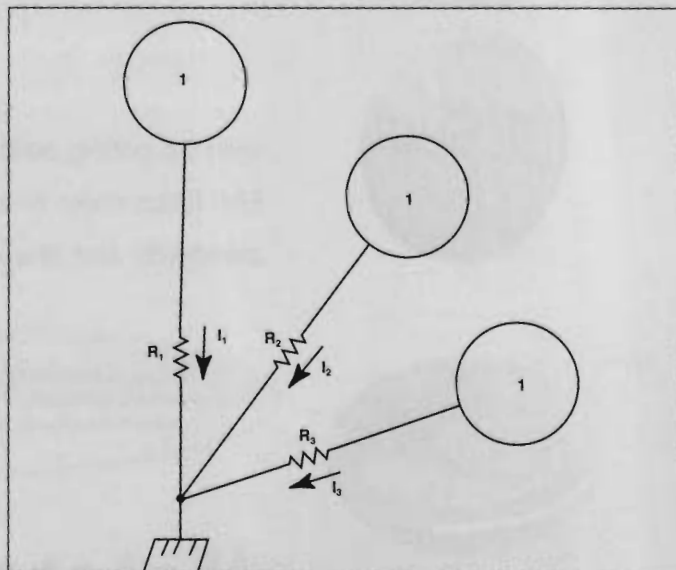


Figure 2b. Single-point grounding scheme avoids local voltage drops .

can affect the functioning of electronic circuits by defining the radiated and conducted electric and magnetic fields in the circuit. Significant reduction in electromagnetic interference can be achieved by following good board layout techniques. Some of the key points to be taken into consideration during the

design cycle are:

- Components on the board should be zoned according to frequency of operation and power levels. Zoning into separate regions is a very economical way to reduce noise effects. The objective is to avoid interference and coupling of fields between adjacent circuits, especially

with high frequency and highly sensitivity circuits.

- Keep analog and digital circuits isolated.
- Trace lengths should be kept as short as possible. A large trace length behaves like a transmission line.
- Traces carrying high frequency signals such as clocks should be routed with minimum number of bends using the shortest trace length to avoid leakage and reflections.
- Avoid sharp turns of tracks such as 90° bends.
- Reduce the overall loop area of the circuit. A large area enclosed by a current loop will cause a higher magnetic field interference. Figures 1a and 1b show different routing examples and the resulting loop areas. One method to reduce loop areas is to have separate ground and power supply planes in multi-layer boards.
- Use filters on input and output lines.
- cross-talk.
- Possible EMI source and victim traces should not run parallel to each other for large distance on the board.
- A ground trace between the possible source and victim traces will considerably reduce the incidence and gravity of the problem of EMI, besides reducing loop area.
- Reduce the possibility of standing waves caused signal reflections by proper impedance matching.
- Provide large ground plane areas on the board.
- Minimize the effect of di/dt in the circuit by using the minimum possible switching frequency required in the design and by reducing the loop area enclosed by the current path.
- Keep high power circuits separated from low power circuits.
- Printed circuit board traces act like transmission lines at higher frequencies. The characteristic impedance of traces having larger width is lower than narrower traces. Parasitic inductance of traces and parasitic capacitance between traces exist in all types of PCBs and could become significant factors at the frequency of operation of the circuit. The properties of the laminate of the PCB such as dielectric constant are significant for transmission line effects and microstrip circuits.
- To prevent leakage of fields, do not place high frequency clocks, oscillator outputs, etc. near I/O points.
- Route high speed clock lines between ground and power supply lines.

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- Reduce cross-talk between adjacent traces by proper spacing, minimizing the length of parallel run between them, routing the source and victim traces on the opposite sides of the ground plane, avoiding sharp bends in the traces, and by providing proper impedance matching.
- Use a low impedance ground in the design so that any electrostatic discharge currents can easily flow to ground without finding other low-impedance paths through electronic devices.
- Route a trace all round the PCB edge and connect it to ground to discharge any static charges due to human contact.
- Route reset lines of microprocessor or other logic devices away from I/O points in the circuit and isolate them.
- Convert unused areas in a PCBs into ground planes. Signal lines should have ground lines running close to them. Multilayer boards with separate ground planes are preferable from ESD point of view.
- Where high frequency clocks are required to interface with components, use a good distribution scheme to directly connect the clock to the components using shortest possible distance. This will prevent radiation leakage of high frequency clocks to nearby circuits which could occur if long traces are used to connect clock signals.
- Coils, transformers and similar elements should be properly shielded to avoid radiating EMI to nearby components and circuits.
- Mount sensitive electronic components away from board edges so that human operators cannot accidentally cause ESD damage while handling the boards.

### Proper grounding techniques to reduce EMI/ESD problems

Proper grounding is an important tool for reducing interference in an electronic system. Although grounding techniques can solve a number of electrical noise and interference problems, faulty grounding can cause the very problems that grounding is supposed to solve. Maintaining a clean ground holds the key to the proper functioning of many electronic circuits using a mixture of analog and digital circuits.

One method of grounding is to have a common ground point from each of the 'local' ground points. A daisy chained ground connection will cause

local circulating currents and hence voltage drops as shown in Fig. 2a. The individual ground points will be at different potentials with respect to each other. If different individual ground points are connected together, they could cause noise problems if the circuit has high power sections. Single point grounding can lead to long ground connections, but it avoids voltage drops across different ground paths and different potentials.

At low frequencies (<1 MHz) the parasitic inductances of the cables, PCB traces, and other interconnecting elements in the circuit do not contribute significantly to any parasitic impedances and, therefore, a single ground point can be used in the circuit (see Fig. 2b). At higher frequencies (>1MHz), the contributing factors for parasitic impedances due to parasitic inductances are many and it is preferable to use a large ground plane, to which the separate grounds are connected.

It is recommended to keep ground connections grouped according to their power and noise levels. One must also take care to avoid ground loops when these individual grounds are formed, preventing circulating currents and the possibility of such loops acting as antennas.

### Proper packaging and production techniques

The effects of electromagnetic and electrostatic fields in a system can be minimized by using a shield of suitable material. The fundamental principle used for shielding a circuit or a system from electromagnetic field interference is reflection and absorption of the incident wave by the shielding material.

The type of shielding used in a particular application depends on the impedance offered by the shielding material at that frequency to the incident electromagnetic field. If the impedance offered by the material to the incident field is matched to the wave impedance of the field, the incident field will be absorbed (maximum power transfer theorem) and very little of the incident field will be reflected.

Ferromagnetic materials such as iron, iron-nickel alloys, mumetal, permalloy, etc. which have high permeability are efficient shielding materials for low-frequency magnetic fields. The permeability of these materials decreases as frequency increases, and at very high frequencies, these conven-

tional magnetic materials will be ineffective as shielding materials.

Non-magnetic materials such as copper or aluminum are applicable to higher frequencies due to their ability to reflect the incident. Efficient shielding against electric fields can be achieved by high conductivity materials such as copper or aluminum. However, such materials cannot be used to shield against magnetic fields because the reflection loss will be negligible.

Some good guidelines for packaging design are:

- Mount a connector inside a cavity so that if a charged body happens to come in contact, it will get discharged through the shielded housing first before any charge transfer occurs to the cable.
- Cover unused connectors with a conductive shield to prevent charge build-up.
- All metallic parts of the system such as cabinet, cable shields, connector shells, etc. which are exposed to the outside world should be grounded.
- Electrical continuity to ground should be maintained at hinges and similar points of the enclosure.
- Avoid long joints and large openings in the enclosure. A discontinuity such as a vent hole in the cabinet can radiate fields. A conductive wire mesh should be mounted on the opening to cover it with smaller size apertures. As a rule any aperture should be less than  $l/20$  wide to avoid leakage through it, where  $l$  is the wave-length of the signal frequency in the system. It is preferable to use many small openings instead of one large opening in the enclosure.
- All non-conductive plastic components mounted on the front panel should have sufficient dielectric strength.
- All components, PCB traces, etc. should be mounted away from any apertures in the enclosure, so that any arcing cannot occur from high voltage ESD pulses coming near the enclosure.

### Dealing with shielding discontinuities

In practice, a system will have openings for cabling, cooling vent holes, cut-outs for fixing switches, hinges for doors, etc. All these discontinuities reduce the shielding effectiveness of the shield used by providing a path for leakage of lines of flux. These holes are more problematic from the point of view of leakage of magnetic field than



electric field. These openings can act like slot antennas and radiate unwanted EMI to the surroundings.

In practice, the radiation will be maximum when the maximum dimension of the opening is equal to  $l/2$  where  $l$  is the wavelength of the signal. Thusly, the maximum length of an aperture should be less than  $l/20$ . A  $60^\circ$  array of holes is reported to reduce the effective hole area. Conductive gaskets, paints, screens, etc. can be used to reduce radiation leakage from openings and to maintain shielding integrity. Cables, wires, etc. entering the enclosure should have a shield which should be fully connected ( $360^\circ$ ) to the enclosure at the entry point.

### Keeping environmental ESD under control

Sources of electric charge in a production set up include personnel, clothing, computer terminals, synthetic packaging materials, furniture coverings, etc. To help minimize ESD from such sources store sensitive components in ESD resistant environments. Plastic surfaces coated with chemicals such as ammonium salts, amidoamines, etc. are available for packing. Containers for storing sensitive components are available in the form of conductive plastic bins, trays, tubes, carbon-filled plastics, metal foil lined bags, etc. ESD control through anti-static flooring is a useful measure as well, with newer materials are now available for flooring, which achieve a conductivity level of  $10^5$  W/sq.

Assembled PCBs should be stored in static dissipative bags during storage and shipment. Such containers are specially coated to achieve the required level of surface resistivity. This allows for the bleed off of charges caused by triboelectric effect and prevent charge accumulation between the pins of the device.

Floor and work table areas should be covered with anti-static material. Use a soldering iron with grounded tip. Tools with plastic handles should be avoided because plastic can become charged from friction. Card rework such as insertion or removal of components with the PCB powered up should be also avoided. Workers should wear anti-static footwear, aprons and wrist bands with proper ground connections. Air ionisers can be used to neutralize free charges in assembly areas. Educate workers in observing ESD precautions

and usage of good work methods to minimize ESD problems.

### Cables—EMI and ESD purgatory

Cables contribute significantly to EMI problems especially in RF systems. Problem areas include connectors, cable length and type of cable used for interconnection and the way the cables are routed around the system. Shielded cables are preferable from EMI reduction point of view. The shield should be connected to the connector with a full  $360^\circ$ , to avoid the "pigtail effect" i. e., a short piece of the shield acting like an antenna. A single point contact through a piece of wire will have a higher inductive reactance at higher frequencies. EMI shielding tapes can be used to wrap cables and reduce EMI problems. For low-frequency ( $< 1$  MHz) electric fields, shield can be grounded at one end, however, for higher frequencies ( $> 1$  MHz), the cable shield should be grounded at both ends. All conductors entering an enclosure should have a shield or filter. All component filters consist of inductors, capacitors and ferrite, should have short lead lengths and be mounted adjacent to entry/exit points. The filter casing should be firmly bonded to the enclosure which should be grounded.

RF designers should be particularly cautious about ESD induced into external cables running to and from the equipment. A piece of cable can act like an antenna to either pick up or radiate a field, and act as a transducer to convert a radiated field into a current or a voltage. Cables without shielding such as untwisted wires, flat cables, etc. are the main types of susceptible cables. The higher the conductivity of the shield, the lower is the sensitivity of the cable to ESD. Such a higher conductivity shield also provides an equipotential surface for the ESD charges and reduces arcing and discharge problems due to potential differences.

Insertion of a common mode choke in the interconnecting cable will help in dropping any voltage developed due to ESD voltages. To protect against very fast transients, bypass capacitors and transient suppressor diodes should be connected across the circuit input terminals to ground. Insertion of filters on the lines will also help in reducing the effects of transient voltages.

Minimize loop areas formed by cables and interconnecting wires. Group

cables according to power level and type of signal carried. Maintain maximum separation between AC and DC cables. Use twisted wires for balanced lines. For unshielded cables use high frequency decoupling which could consist of a T-S filter having two ferrite beads and a ceramic capacitor of about 100 pF so that high frequency noise induced by ESD is filtered out.

### Thermal issues

Thermal design is as important as the design of the electronics and this aspect should be addressed at the design stage of a system to prevent problems surfacing later on in the field under adverse environmental conditions of temperature, humidity, etc. Manufacturers of semiconductor devices generally specify the maximum range of junction temperature for continuous operation to be  $125^\circ\text{C}$  to  $150^\circ\text{C}$ . However, in order to achieve high reliability of operation, the junction temperature should be maintained as low as possible ( $< 100^\circ\text{C}$ ). This can be achieved by providing heat sinks, cooling fans, blowers, etc., based upon the amount of heat generated and the cooling desired. The three fundamental mechanisms of heat transfer; conduction, convection, and radiation are all equally important. Each one plays a significant role in a different layer in the thermal management hierarchy and should be considered during the thermal design of any electronic system.

In places where ambient temperatures are much higher than the typical room temperature of  $25^\circ\text{C}$ , the thermal environment becomes far more critical and the power dissipation rating of the device should be derated appropriately.

The term thermal overstress includes factors responsible for device failure due to excessive heat dissipation beyond the safe heat dissipation limits of the device. Thermal overstress manifests itself in the failure of an integrated circuit in the form of charring of the device, melting of bonding wires, carbonation of the plastic encapsulating material. Some of the ways by which thermal overstress manifests itself are:

- Thermal fatigue—This is caused by switching action. It is seen as cracking and fracturing of a device due to differential thermal expansion and contraction between the different materials used.
- Thermal runaway—Under some conditions, a semiconductor device will

have a multiplier effect due to a positive feedback mechanism where an increase in device current leads to higher power dissipation in a repetitive chain reaction. This will lead to the destruction of the device due to the excessive heat generated by such a reaction.

- **Hot Spots**—Any defect in a semiconductor device or improper provision for conducting the heat away from a device can cause hot spots in the device due to accumulation of heat in a particular spot even during normal operation and this can cause damage to the device. Hot spot related failures can occur not only in semiconductor devices but also in other components such as transformers, coils, capacitors, resistors, etc.

- **Thermal problems on the PCB** - The possible sources of heat generation on the populated PCB could be power transistors, high power resistors (such as wire wound types), transformers, power diodes, power MOSFETs, etc. Power devices such as power transistors are mounted on heat sinks to carry away the heat from the device and prevent abnormal rise in temperature. Heat transfer can occur from a hot device to another device on the board by any or all of the three fundamental heat transfer mechanisms - conduction, convection and radiation. Conductive heat transfer can occur through the lead of the power device to the PCB traces where the leads are soldered, which transfers to other components through interconnecting traces. Excessive temperature during soldering can cause damage to a PCB as well. In general, the effects of thermal stresses on a PCB are delamination, discoloration, warping, and in extreme cases, charring of the board.

Generally, components can withstand thermal shocks encountered during normal assembly/production operations such as soldering. It is only the sustained application of thermal stresses beyond the specifications of the component that will cause the device to malfunction or fail due to thermal mechanisms. For high reliability systems, screening tests are conducted to weed out infant mortality failures by conducting temperature cycling tests.

The following steps can be followed to achieve good thermal design:

- Proper placement of components on the board is critical. Components generating heat such as power devices, high power resistors, etc. should be mounted away from other components

especially those sensitive to heat such as electrolytic capacitors, semiconductor devices, etc.

- Provide adequate heat sink for power dissipating components and provide baffles, if required, for better air circulation.

- Since hot air has lower density and rises up, cool air should be passed from the bottom so that it gets heated and rises up.

- Any dust filters used in the system cabinet should be kept clean to ensure proper air passage.

- Provide cooling fans for assisted air movement.

### Conclusion

The demand for light-weight, compact and highly integrated devices has been increasing in the recent years. This tight integration of electronic components and packaging creates a new era of EMI and ESD problems. Incorporating good thermal design and maintaining EMI/ESD compliance within a small volume becomes a challenging task. Techniques to overcome these problems should include better circuit, PCB and system design, packaging, shielding, and application of cooling techniques.

Devices based on new technology and having built-in protection against ESD/EMI damage, and packaging materials to overcome EMI/ESD problems are now available.

Compactness of product design requires trade-offs in power dissipation, EMI/ESD susceptibility and emission, space constraints and cost of the product. Application of the various techniques can contribute significantly to the reduction of EMI, ESD and thermally caused failures of electronic components.

By integrating the various requirements in terms of standards and compliance right from the design stage of a system, the problem of EMI/ESD compliance and thermal design can be tackled at a lower cost. If sufficient precautions are not taken during the product development cycle, achieving EMC/ESD compliance may not be possible without expensive re-engineering or retrofits. Moreover, the product may have higher incidence of field related problems and failures and valuable time and effort will be lost for fixing them later.

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Biography :

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